REMARKS

Reconsideration and allowance of the subject application are respectfully requested. Claims 1-10 are all the claims pending in the application. In response to the Office Action, Applicant respectfully submits that the claims define patentable subject matter.

I. Overview of the Office Action

Claim 1 remains rejected under 35 U.S.C. § 103(a) as being unpatentable over Bourke et al. (U.S. Patent No. 5,509,124, hereafter "Bourke") in view of Barrenscheen et al. (U.S. Patent Application Publication No. 2003/0084226, hereafter "Barrenscheen"). Claims 2-6 remain rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki et al. (JP 2000-92365A, hereafter "Masayuki") in view of Barrenscheen. Claims 7-9 remain rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen, and further in view of Sodos (U.S. Patent No. 5,239,651). Claim 10 remains rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen and Luo et al. (U.S. Patent No. 6,265,885, hereafter "Luo").

II. Preliminary Matters

Applicant respectfully traverses the rejections and submits that Barrenscheen does not qualify as prior art under 35 U.S.C. § 103(a) with respect to the present application. Applicant submits herewith a Declaration under 37 C.F.R. § 1.131 demonstrating conception and diligence leading to constructive reduction to practice of the instant invention prior to the earliest effective filing date of Barrenscheen, October 31, 2002. In Particular, Applicant submits the following:

(a) An executed Declaration under Rule 1.131, which states that the invention was conceived prior to October 31, 2002. Clearly, Applicants acted with due diligence from prior to October 31, 2002 by filing Korean Application No. 10-2003-0003471 on January 18, 2003 (in the Exhibit attached to the Declaration, information not related to the issue of the diligence have been blocked off as permitted by MPEP 715.07 II);

(b) Documents 1-6 show Applicant's diligence from October 16, 2002 to January 18, 2003 in filing Korean Application No. 10-2003-0003471.

(c) A translated copy of an In-Service Invention Report (Exhibit A) wherein the inventor's date of the report is October 16, 2002, and the Patent Department receipt date is October 16, 2002, wherein Korean Application No. 10-2003-0003471 was filed shortly thereafter on January 18, 2003 as the priority application for the present application.

Since the In-Service Invention Report (Exhibit A) and Documents 1-6 demonstrate that Applicant was actively preparing the Korean Application No. 10-2003-0003471 prior to October 31, 2002, the earliest U.S. filing date of Barrenscheen, Applicant submits that the foregoing documents clearly provide evidence of conception of the present invention prior to October 31, 2002, which is the earliest effective filing date of Barrenscheen, together with due diligence from prior to October 31, 2002 to January 18, 2003, the filing date of the priority document of the present application.

Therefore, removal of Barrenscheen as a reference is respectfully requested. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection be withdrawn.

III. Prior Art Rejections

In the previous Office Action dated June 26, 2006, the Examiner asserted that Barrenscheen discloses "the multiplexer receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor" as recited in independent clam 1, and cited the claimed multiplexer as allegedly reading on Bus Interface (BI1)

In the Response filed on October 26, 2006, Applicant submitted that the Bus Interface BI1 is not a multiplexer. Instead, Bus Interfaces BI1-BI4 are used to connect the data transmission device DTU to the first through fourth buses BUS1-BUS4, respectively. Consequently, Bus Interface BI1 does not perform the functions of and is not described as a multiplexer in Barrenscheen.

In response, the Examiner maintains that the claimed multiplexer reads on the Bus Interface (BI1), and asserts that:

> [T]he recited claiming language "multiplexer," and its function in the exemplary claim 1 are interpreted as the bus interface BI1 performs the functions of and is described as the claimed subject matter "multiplexer" in Barrenscheen.[1]

[1] Page 17 of the Office Action dated January 18, 2007.

Applicant respectfully submits that claim 1 would not have been rendered obvious by Bourke and Barrenscheen. There is simply no disclosure in Barrenscheen that the Bus interface, BI1 acts as or performs the functions of a multiplexer.

The Examiner also maintains that Barrenscheen discloses that BUS1 is synchronized with the processor, and cites paragraph [0035] of Barrenscheen as allegedly disclosing this feature of claim 1. However, paragraph [0035] merely discloses that when the data transmission device (DTU) is used as a DMA controller, it can transmit data between devices connected to the same bus or between devices connected between different buses autonomously. There is simply no disclosure in Barrenscheen that the BUS1 is synchronized with a processor.

In the previous office Action, the Examiner asserted that Masayuki teaches both a synchronous bus and an asynchronous bus as required by independent claims 2, 4, and 10, and cited bus 34 and bus 33 of Masayuki as allegedly respectively reading on the claimed synchronous and asynchronous buses.

In the October 26, 2006 Response, Applicant submitted that it appeared that the Examiner was merely assuming that CPU bus 34 is (synchronous) synchronized with CPU 41, and that image data bus 33 is (asynchronous) not synchronized with CPU 41 because image data bus 33 is not directly connected to CPU 41 in Fig. 2. However, nowhere does Masayuki disclose that image data bus 33 is asynchronous. Moreover, Masayuki does not disclose any terms related to "synchronous" and "asynchronous".

In response, the Examiner simply asserts that:

> Even though the Applicant argues that Masayuki does not disclose any terms related to 'synchronous' and 'asynchronous', Masayuki discloses CPU (i.e., processor) and CPU bus (i.e., synchronized bus with said CPU), and further, image data bus (i.e., asynchronous data bus) being synchronized by Sync Generator in the Signal Processor, not being synchronized with said CPU (i.e., processor).[2]

Further, the Examiner continues to assert that Masayuki inherently suggests that the image data bus (Bus 33) is not synchronized with the CPU.

Applicant respectfully submits that claim 2 and analogous claims 4 and 10 would not have been rendered obvious over Masayuki.

First, there is simply no teaching or suggestion in Masayuki of synchronous and asynchronous buses. Masayuki teaches a method of preventing delays on an image data bus and improving signal processing efficiency by controlling/managing the read-out and write-in process of storage means connected to the image data bus. Nowhere does Masayuki disclose synchronizing a data bus with a processor. The fact that Masayuki teaches a signal processing unit which prevents delay of image data does not necessarily mean that this "inherently" teaches that the image data bus is synchronized with the CPU as alleged by the Examiner.[3]

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[2] Pages 18-19 of the Office Action dated January 18, 2007.

[3] Page 19 of the Office Action dated January 18, 2007.

Second, the comments in the Office Action regarding inherency are not understood; the principle of inherency is applicable only with respect to 35 U.S.C. §102 rejections. Inherency and obviousness are distinct concepts. A retrospective view of inherency is not a substitute for some teaching or suggestion that supports the selection and use of the elements in the particular claimed combination. In deciding that a novel combination would have been obvious, there must be a supporting teaching in the prior art; for that which may be inherent is not necessarily known, and obviousness cannot be predicated on what is unknown. See In re Newell, 13 U.S.P.Q.2d 1248, 1250 (Fed. Cir. 1989).

Accordingly, Applicant respectfully submits that independent claims 1, 2, 4, and 10 as well as dependent claims 3, and 5-9 should be allowable because the cited references do not teach or suggest all of the features of the claims.

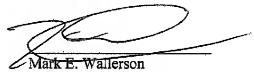
In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Applicant files concurrently herewith a Petition (with fee) for an Extension of Time of one month, thereby extending the time for response to **May 18, 2007**. Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this application, and any required fee for such extension is to be charged to Deposit Account No. 19-4880. The Commissioner is also authorized to charge any additional fees under 37 C.F.R. § 1.16 and/or § 1.17

necessary to keep this application pending in the Patent and Trademark Office or credit any overpayment to said Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Mark E. Wallerson
Registration No. 59,043

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

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